**ASHOK L**

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**Objective:**

To pursue a challenging career in the field of **software** and to contribute and enhance my technical skills.

**Summary:**

* 3+ year of experience in VLSI front end design, Embedded Systems design and development, and Embedded Linux
* Experience in VHDL, and VerilogHDL programming
* Hands on experience on Xilinx tool, and QuestaSim tool
* Experience in debugging using Chip Scope Pro, and FPGA validation
* Experience in AHB Bus protocol, AXI, SPI and I2C
* Experience in debugging Techniques gdb, strace, valgrind
* Worked on Source Code version Control Tool (GIT)
* Experience in Linux System Programming
* Experience in Communication protocols like I2C, SPI, and UART
* Proficient in C programming and Python
* Knowledge on Shell Scripting

**Technical Proficiency:**

**Programming Languages:** VHDL, VerilogHDL, and C.

**Scripting Languages**: Shell, and Python.  
**Simulation & Synthesis Tools**: Xilinx ISE 9.2i, Xilinx ISE 13.2i, and Mentor Graphics tool suite (QuestaSim, ModelSim).  
**FPGA Boards**: Xilinx Spartan 3E (500E, 1200E), Basys 100E.  
**Bus Architectures**: AHB Bus protocol, AXI, SPI and I2C.

**FPGA Validation Tools:** Knowledge on debugging using Chip Scope Pro. Have experience in FPGA validation.  
**Applications**: MS Office.  
**Operating Systems:** Linux, Windows 7.

**Technical Experience:**

* Czech Technology Pvt Ltd, Hyderabad, October-2011 to April-2012 as a

**Project trainee.**

* Simpli5NG Semiconductor Pvt Ltd, Hyderabad, May-2012 to October-2014 as a

**Digital Design Engineer**

* VotaryTech soft solutions Pvt Ltd, Hyderabad, Aug-2016 to Till now as a

**Software Engineer.**

Educational Profile:

Nov 2014 - Aug 2016 JNTUH College of Engineering karimnagar, **Master, DSCE**

Aug 2007 - Jun 2011 Maheshwara Engineering College, **Bachelor, ECE**

June 2005 - May 2007 St. Anthony’s Junior College, **Associate, MPC**

June 2004 - May 2005 GOVT HIGH SCHOOL Sadasivpet, High School

**Projects:**

**Project 1: IoT Based Alert System**

Role : Team Member

Hardware Platform : ARM Cortex-A53

Development Tools : Linux 3.8, GCC tool chain, SCONs

Platform : Linux

**Description**:

When ever Developer Pushes New Build to Version Control, Build & Integration tool like Jenkins will detect and build, on build FAIL it sends e-mail to Client(Remote Device) through pre-configured e-mail id. Here client is raspberry pi, which is pre-configured with IMAP e-mail client to read received e-mail’s, upon receiving Build FAIL e-mail from B&I Tool should trigger alarm/flash on screen.

**Roles & Responsibilities:**

* Preparation of SRS doc
* Preparation of Detailed design document
* Developed python code for Client application

**Project 2: VITA (**VotaryTech IOT Architecture) Project

Role : Team Member

Hardware Platform : ARM Cortex-A53

Development Tools : Linux 3.8, GCC tool chain, SCONs

Platform : Linux

**Description**:

DM is IoT-Gateway software designed in RestFull Architecture. It acquires heterogeneous datasets from multiple sensors and converts them to a standard format that is understood by the next stage of the data processing pipeline. I was involved in design and development of DM connectivity layer which abstracts Connectivity technologies like BLE(bluez3.57), IP.

**Roles & Responsibilities:**

* Design development of connectivity module using Bluez source code
* Design and Implementation API’s for client application
* Testing the API’s with an simple application
* Preparing the documentation for the project

**Project3: AHB Memory Interface**

**Description:**

The memory controller is the part of the system that controls the memory. It generates the necessary signals to control the reading and writing of information from and to the memory, and interfaces the memory with the other major parts of the system.

**Role**:

* Developed micro-architecture for AHB Slave Interface.
* Developed RTL for AHB Slave Interface in **VerilogHDL.**

**Project4: MCP interconnect bus.**

**Description:**

The Multicast communication protocol is to transfer the data from source node to destination node in the multilayer network. The routing has built in intelligence to transfer the data with least path from source to destination. The design consists of Routing Mode (RM), Communication Mode (CM), and Number of Destinations on the Bus (NDB).

**Role:**

* Developed RTL for routing logic in **VHDL**.
* Debugging the RTL on FPGA (**ISE chip scope pro**) using different test cases.